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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/902,140	07/10/2001	Karl-Eugen Kroell	DE9-2000-0026	7994

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INTERNATIONAL BUSINESS MACHINES CORPORATION
DEPT. 18G
BLDG. 300-482
2070 ROUTE 52
HOPEWELL JUNCTION, NY 12533

EXAMINER
JONES, HUGH M

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 06/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/902,140	Kroell et al.
Examiner	**Art Unit**
Hugh Jones	2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Jul 10, 2001* .

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-14* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☒ All b) ☐ Some* c) ☐ None of:

1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 2
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Introduction

1. Claims 1-14 of U. S. Application 09/902,140 filed on 07-10-2001, are presented for examination.

Claim Objections

2. The following is a quotation of 37 C.F.R. § 1.75 (d)(1):

> The claim or claims must conform to the invention as set forth in the remainder of the specification and terms and phrases used in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description.

3. Claims 1-14 are objected to because of the following.

- claim 2, 8, 10, 12, 14 refer to "putting out". The Examiner makes the assumption that this means "outputting". Please make the appropriate corrections.

- The independent claims are objected to because of the following informalities: the first limitation recites "...at the ***begin*** of a functional cycle..." Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 3-4 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to

one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

- Applicants have disclosed insufficient detail pertaining to "automatically correcting dynamic errors in the simulation input file", as recited in claims 3-4, for example, in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

6. **Claims 3-4 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.**

- Applicants have described, in the specification, "automatically correcting dynamic errors in the simulation input file", as recited in claims 3-4, for example, in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Double Patenting

7. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ

761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

8. A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

9. Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

10. Claims 1-14 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-19 of U.S. Patent No. 6,442,735 in view of Dangelo et al. (US Patent 5,555,201). Although the conflicting claims are not identical, they are not patentably distinct from each other for the following reasons. The patented claims refer to an "object list" in apparent reference to object oriented concepts while the pending claims do not refer to object classes. Dangelo et al. discloses use of object-oriented circuit simulation wherein the means for circuit simulation may include one or more general purpose computers interfaced to the ECAD system's computer, one or more hardware simulators interfaced to the ECAD system's computer, or any combination of these. The user interacts with the ECAD system through the use of an object-oriented user interface, whereby the user may create, select, move, modify and delete objects on the display screen, where objects may represent circuit components, wires, commands, text values, or any other visual representation of data. The graphical and software techniques of interacting with a

user on such an object-oriented user interface are well known to those skilled in the art and need not be elaborated upon in this discussion. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Joshi et al. with the teachings of Dangeo et al. because of the ease of use of such techniques - see Dangelo et al. (Col. 3, lines 45-56), "Typically, the form of user interaction with the schematic editor is an object-oriented screen display whereby the user thereof may manipulate objects on the screen through the use of a pointing device. A pointing device is any device through the use of which a user may "point" to and identify objects on a display screen. Such object-oriented interfaces are well known to those skilled in the art. One example of such and interface is the Macintosh Finder for the Apple Macintosh computer, both produced by Apple Computer, Inc."

Claim Rejections - 35 USC § 101

11. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

12. Claims 9-12 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claims 9-12 appear to recite a computer program product. It should be noted that code (i.e., a computer software program) does not do anything per se. Instead, it is the code stored on a computer that, *when executed*, instructs the computer to perform various functions. The following claim is a generic example of a proper computer program product claim;

13. A computer program product embodied on a computer-readable medium and comprising code that, when executed, causes a computer to perform the following:

Function A

Function B

Function C, etc..

Claim Interpretations

14. The broadest reasonable interpretation has been given to the claims. The Examiner interprets that static error corresponds to the DC-simulation and that dynamic error corresponds to the transient analysis. The Examiner further interprets that the transient analysis is also carried out on the same exact circuit and with the same conditions.

Claim Rejections - 35 USC § 102

15. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

16. A person shall be entitled to a patent unless -

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

17. Claims 1, 5, 7, 9, 11, 13 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Wong (US Patent 4,918,643) or Wong et al. (IEEE - 1997).

18. Wong (US Patent 4,918,643) discloses a method of accelerating the pace at which circuit simulators are able to converge to a steady state solution of a periodic piecewise-linear system or periodically driven piecewise-linear system transforms the problem into finding the solution of a nonlinear function in terms of a state vector, which is then solved by a truncated power series such as the Newton-Raphson iterative procedure. Usage of this method requires the determination of system sensitivity with respect to the state vector. This system sensitivity is determined by solving for the sensitivity of the state vector at the exit of each subinterval of the periodic cycle with respect to the state vector at the entry of the same subinterval. This sensitivity is accurately resolved by considering the sensitivity of the time duration spent in this subinterval with respect to the state vector at the entry of the same subinterval. The sensitivity of time duration is factored into the computation process by computing a subinterval Jacobian matrix for each subinterval. This subinterval Jacobian matrix is computed by adding a subinterval correction matrix to a subinterval state transition matrix to account for changes in subinterval time duration. The cyclic Jacobian matrix for the entire periodic cycle is computed and utizlied in an iteration procedure to adjust a value of the initial state vector. *In particular, Wong discloses DC analysis with error detection and correction - see fig. 2, 3-4, 13; col. 2, lines 7-33; col. 3, line 23 to col. 5, line 14; col. 11-12.*

19. Wong et al. (IEEE - 1997) discloses "*Accelerated steady-state analysis technique for PWM DC/DC switching regulators.*" Wong et al. further disclose an iterative technique for steady-state

analysis of PWM DC/DC switching regulators. The algorithm consists of two iteration loops. The first one is to iterate the steady-state network waveforms at a presumed duty cycle while the second one is to iterate the steady-state duty cycle of the pulse-width modulator output. The circuit waveforms are obtained by a stepwise time domain simulation method, which is based on using stepwise quadratic formulations of the circuit stale variables with progressive analysis of switches' state. *In particular, Wong et al. discloses DC analysis with error detection and correction - see fig.* 2-3 and corresponding text.

20. Claims 1-14 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Joshi et al. (US Patent 6,442,735).

21. Joshi et al. disclose a computer program product method of circuit design of a multiple input circuit, macro or chip, especially for silicon on insulator (SOI) circuits. For a multiple input circuit, an object list of items corresponding to circuit devices is created. The items model local effects on corresponding circuit elements. ***The circuit is analyzed using Static or DC analysis to provide initial local effects on circuit devices, including body effects and local heat effects. The initial local effects are passed to the circuit model for transient analysis. The local effects from checked transient results are checked and updated. The transient response is rerun and the local effects are updated until the change in local effects is below an upper limit.*** For added efficiency, unswitching devices may be eliminated from the iterative analysis and analysis may be limited to the period when switching occurs. Note figure 2 and corresponding text, including DC analysis, use of

macro and cover models to edit the static error, transient analysis and, again, use of macro and cover model to edit errors.

Claim Rejections - 35 USC § 103

22. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

23. The factual inquiries set forth in *Graham v. John Deere Co.*, 148 USPQ 459, that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or unobviousness.

24. Claim 1-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto in view of Wong (US Patent 4,918,643) or Wong et al. (IEEE - 1997).

25. Sakamoto discloses: "FIG. 2 is a flowchart illustrating this second prior art. In a step S21, circuit information is input, and in a step S22, a time Tcal for calculating the eigenvalue is read. **In succeeding steps S23 and S24, a circuit matrix is prepared, and a *DC analysis* is carried out.**

In a step S25, ***a transient analysis is conducted,*** and when the analysis time becomes the time Tcal, matrix data is written into a magnetic disk. After a series of steps (S31 to S36) for the transient analysis are completed, a step S26 for processing the eigenvalue display is conducted. In brief, the matrix data is read out (step S37), and the eigenvalue is calculated on the basis of the read-out matrix data (step S38). A real-number part and an imaginary-number part of the calculated eigenvalue are displayed on an X coordinate axis and a Y coordinate axis, respectively (step S39)."

26. Thus, Sakamoto discloses a steady-state simulation followed by a transient simulation (fig. 3 and corresponding text).

27. Sakamoto does not expressly disclose checking the simulations for errors and then correcting the errors. Wong or Wong et al. disclose checking simulations to ensure accuracy and correcting the simulations when the error is deemed significant.

28. Wong (US Patent 4,918,643) discloses a method of accelerating the pace at which circuit simulators are able to converge to a steady state solution of a periodic piecewise-linear system or periodically driven piecewise-linear system transforms the problem into finding the solution of a nonlinear function in terms of a state vector, which is then solved by a truncated power series such as the Newton-Raphson iterative procedure. Usage of this method requires the determination of system sensitivity with respect to the state vector. This system sensitivity is determined by solving for the sensitivity of the state vector at the exit of each subinterval of the periodic cycle with respect to the state vector at the entry of the same subinterval. This sensitivity is accurately resolved by considering the sensitivity of the time duration spent in this subinterval with respect to the state

vector at the entry of the same subinterval. The sensitivity of time duration is factored into the computation process by computing a subinterval Jacobian matrix for each subinterval. This subinterval Jacobian matrix is computed by adding a subinterval correction matrix to a subinterval state transition matrix to account for changes in subinterval time duration. The cyclic Jacobian matrix for the entire periodic cycle is computed and utizlied in an iteration procedure to adjust a value of the initial state vector. *In particular, Wong discloses DC analysis with error detection and correction - see fig. 2, 3-4, 13; col. 2, lines 7-33; col. 3, line 23 to col. 5, line 14; col. 11-12.*

29. Wong et al. (IEEE - 1997) discloses "*Accelerated steady-state analysis technique for PWM DC/DC switching regulators.*" Wong et al. further disclose an iterative technique for steady-state analysis of PWM DC/DC switching regulators. The algorithm consists of two iteration loops. The first one is to iterate the steady-state network waveforms at a presumed duty cycle while the second one is to iterate the steady-state duty cycle of the pulse-width modulator output. The circuit waveforms are obtained by a stepwise time domain simulation method, which is based on using stepwise quadratic formulations of the circuit stale variables with progressive analysis of switches' state. *In particular, Wong et al. discloses DC analysis with error detection and correction - see fig.* 2-3 and corresponding text.

30. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Sakamoto with the teachings of Wong or Wong et al. to obtain the claimed invention for the following reasons. Steady-state and transient simulations are not very useful or realistic if they are not accurate.

Conclusion

31. Any inquiry concerning this communication or earlier communications from the examiner should be:

directed to: Dr. Hugh Jones telephone number (703) 305-0023, Monday-Thursday 0830 to 0700 ET, ***or*** the examiner's supervisor, Kevin Teska, telephone number (703) 305-9704. Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist, telephone number (703) 305-3900.

mailed to: Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to: (703) 308-9051 (for formal communications intended for entry) ***or***
(703) 308-1396 (for informal or draft communications, please label "*PROPOSED*" or "*DRAFT*").

Dr. Hugh Jones

Primary Patent Examiner

June 2, 2003

HUGH JONES/Ph.D.
PRIMARY PATENT EXAMINER
TECHNOLOGY CENTER 2100